03-31-05

PTO/SB/21 (09-04)

OIPE JC10 MAR 29 2005 PATENT & TRADEMARK OFFICE

TRANSMITTAL FORM

(to be used for all correspondence after initial filing)

Total Number of Pages in This Submission: 15

Application Number	10/826,471
Filing Date	April 16, 2004
First Named Inventor	HOSOYA, Mutsumi
Art Unit	2182
Examiner Name	Unassigned
Attorney Docket Number	16869S-114200US

ENCLOSURES *(Check all that apply)*

- ☒ Fee Transmittal Form
  - ☐ Fee Attached
- ☐ Amendment/Reply
  - ☐ After Final
  - ☐ Affidavits/declaration(s)
- ☐ Extension of Time Request
- ☐ Express Abandonment Request
- ☐ Information Disclosure Statement
- ☐ Certified Copy of Priority Document(s)
- ☐ Reply to Missing Parts/ Incomplete Application
  - ☐ Reply to Missing Parts under 37 CFR 1.52 or 1.53
- ☐ Drawing(s)
- ☐ Licensing-related Papers
- ☒ Petition to Make Special
- ☐ Petition to Convert to a Provisional Application
- ☐ Power of Attorney, Revocation Change of Correspondence Address
- ☐ Terminal Disclaimer
- ☐ Request for Refund
- ☐ CD, Number of CD(s) _____
  - ☐ Landscape Table on CD
- ☐ After Allowance Communication to TC
- ☐ Appeal Communication to Board of Appeals and Interferences
- ☐ Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- ☐ Proprietary Information
- ☐ Status Letter
- ☒ Other Enclosure(s) (please identify below):
  - Return Postcard
  - Eleven (11) cited references

Remarks The Commissioner is authorized to charge any additional fees to Deposit Account 20-1430.

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Townsend and Townsend and Crew LLP		
Signature			
Printed name	Chun-Pok Leung		
Date	March 29, 2005	Reg. No.	41,405

CERTIFICATE OF TRANSMISSION/MAILING

Express Mail Label: **EV 530888138 US**

I hereby certify that this correspondence is being deposited with the United States Postal Service with "Express Mail Post Office to Address" service under 37 CFR 1.10 on this date **March 29, 2005** and is addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450 on the date shown below.

Signature			
Typed or printed name	Joy Salvador	Date	March 29, 2005

PTO/SB/17 (12-04)

Effective on 12/08/2004.
Fees pursuant to the Consolidated Appropriations Act, 2005 (H.R. 4818).

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) **130.00**

Complete if Known	
Application Number	10/826,471
Filing Date	April 16, 2004
First Named Inventor	HOSOYA, Mutsumi
Examiner Name	Unassigned
Art Unit	2182
Attorney Docket No.	16869S-114200US

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order ☐ None ☐ Other (please identify): _____

☒ Deposit Account Deposit Account Number: 20-1430 Deposit Account Name: Townsend and Townsend and Crew LLP

For the above-identified deposit account, the Director is hereby authorized to: (check all that apply)

☒ Charge fee(s) indicated below ☐ Charge fee(s) indicated below, **except for the filing fee**

☒ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17 ☒ Credit any overpayments

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038

FEE CALCULATION

1. BASIC FILING, SEARCH, AND EXAMINATION FEES

Application Type	FILING FEES Fee ($)	FILING FEES Small Entity Fee ($)	SEARCH FEES Fee ($)	SEARCH FEES Small Entity Fee ($)	EXAMINATION FEES Fee ($)	EXAMINATION FEES Small Entity Fee ($)	Fees Paid ($)
Utility	300	150	500	250	200	100	
Design	200	100	100	50	130	65	
Plant	200	100	300	150	160	80	
Reissue	300	150	500	250	600	300	
Provisional	200	100	0	0	0	0	

2. EXCESS CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20 or, for Reissues, each claim over 20 and more than in the original patent	50	25
Each independent claim over 3 or, for Reissues, each independent claim more than in the original patent	200	100
Multiple dependent claims	360	180

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____	-20 or HP = _____	x _____	= _____

HP = highest number of total claims paid for, if greater than 20

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____	-3 or HP = _____	x _____	= _____

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims Fee ($)	Fee Paid ($)
_____	_____

3. APPLICATION SIZE FEE

If the specification and drawings exceed 100 sheets of paper, the application size fee due is $250 ($125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

Total Sheets	Extra Sheets	Number of each additional 50 or fraction thereof	Fee ($)	Fee Paid ($)
_____ - 100 =	_____ / 50 =	_____ (round up to a whole number) x	_____	= _____

4. OTHER FEE(S)

	Fees Paid ($)
Non-English Specification, $130 fee (no small entity discount)	
Other: PETITIONS TO THE COMMISSIONER	130.00

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 41,405	Telephone 650-326-2400
Name (Print/Type)	Chun-Pok Leung		Date March 29, 2005

60455168 v1

PATENT
Attorney Docket No.: 16869S-114200US
Client Ref. No.: W1578-01

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

MUTSUMI HOSOYA *et al.*

Application No.: 10/826,471

Filed: April 16, 2004

For: DISK CONTROLLER

Customer No.: 20350

Examiner: Unassigned

Technology Center/Art Unit: 2182

Confirmation No.: 1494

PETITION TO MAKE SPECIAL FOR NEW APPLICATION UNDER M.P.E.P. § 708.02, VIII & 37 C.F.R. § 1.102(d)

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This is a petition to make special the above-identified application under MPEP § 708.02, VIII & 37 C.F.R. § 1.102(d). The application has not received any examination by an Examiner.

(a) The Commissioner is authorized to charge the petition fee of $130 under 37 C.F.R. § 1.17(i) and any other fees associated with this paper to Deposit Account 20-1430.

(b) All the claims are believed to be directed to a single invention. If the Office determines that all the claims presented are not obviously directed to a single invention, then Applicants will make an election without traverse as a prerequisite to the grant of special status.

(c) Pre-examination searches were made of U.S. issued patents, including a classification search, a foreign patent database search, and a literature search. The searches were performed on or around February 25, 2005, and were conducted by a professional search firm, Mattingly, Stanger & Malur, P.C. The classification search covered Class 710 (subclasses 33, 38, 56, and 58) and Class 711 (subclasses 113, 114, 148, and 154). Because of the large size of these subclasses, keywords were used to narrow of number of documents returned. The foreign patent database search was conducted using Espacenet database and Japanese patent database. Two additional references (see references #8-9) were cited in corresponding foreign applications. The inventors further provided two references (see references #10-11). These were cited in the Information Disclosure Statements filed on April 16, 2004; November 2, 2004; and March 15, 2005.

(d) The following references, copies of which are attached herewith, are deemed most closely related to the subject matter encompassed by the claims:

(1) U.S. Patent No. 5,206,943;

(2) U.S. Patent No. 6,401,149;

(3) U.S. Patent No. 6,604,155;

(4) U.S. Patent Publication No. 2002/0087751 A1;

(5) U.S. Patent Publication No. 2003/0131192 A1;

(6) U.S. Patent Publication No. 2003/0182516 A1;

(7) U.S. Patent Publication No. 2004/0139365 A1;

(8) U.S. Patent No. 5,974,058;

(9) European Patent Publication No. EP 1353264 A2;

(10) U.S. Patent Publication No. 2003/0046460 A1; and

(11) U.S. Patent No. 6,601,134.

(e) Set forth below is a detailed discussion of references which points out with particularity how the claimed subject matter is distinguishable over the references.

A. Claimed Embodiments of the Present Invention

The claimed invention, as set forth in independent claims 1, 7, 8, 22, and 24, is generally directed to a disk controller that uses connection-less multiplex communication. Under independent claim 1, the invention is a disk controller including a channel adapter having a connection interface to a host computer or a disk drive. A memory adapter is included for temporarily storing data to be transferred between the host computer and the disk drive. Also included are a processor adapter for controlling operations of the channel adapter and the memory adapter, and a switch adapter for configuring an inner network by interconnecting the channel adapter, the memory adapter and the processor adapter. The channel adapter, the memory adapter, the processor adapter, and the switch adapter each include a DMA controller for performing communication protocol control of the inner network, and packet multiplex communication is performed among the DMA controllers provided in the adapters.

Additionally, as set forth in independent claim 7, the invention is a disk controller including a channel adapter having a connection interface to a host computer or a disk drive. A memory adapter is included for temporarily storing data to be transferred between the host computer and the disk drive. Also included are a processor adapter for controlling operations of the channel adapter and the memory adapter, and a switch adapter for configuring an inner network by interconnecting the channel adapter, the memory adapter and the processor adapter. The channel adapter, the memory adapter, the processor adapter, and the switch adapter each include a plurality of DMA controllers for performing a communication protocol control of the inner network and one or more data link engines shared by the DMA controllers. The DMA controllers include a plurality of reception FIFO buffers and a plurality of transmission buffers, with one data link engine being made in correspondence with a plurality of buffers. Contention of reception data is arbitrated among respective reception FIFO buffers belonging to a plurality of DMA controllers, and contention of transmission data is arbitrated among respective transmission FIFO buffers

belonging to a plurality of DMA controllers, to thereby set a priority order of a plurality of buffers. A control system inner network and a data system inner network are mixed in one data link engine, and packet multiplex communication is performed among the DMA controllers provided in the adapters.

Furthermore, as set forth in independent claim 8, the invention is a disk controller including a channel adapter having a connection interface to a host computer or a disk drive. A memory adapter is included for temporarily storing data to be transferred between the host computer and the disk drive. Also included are a processor adapter for controlling operations of the channel adapter and the memory adapter, and a switch adapter for configuring an inner network by interconnecting the channel adapter, the memory adapter and the processor adapter. The channel adapter, the memory adapter, the processor adapter, and the switch adapter each include a DMA controller for performing communication protocol control of the inner network. A packet to be transferred among the DMA controllers provided in the adapters has an address field for designating a targeting DMA controller, an address field for designating an initiating DMA controller, and a DMA sequence field for managing a transfer order when on DMA transfer is divided into a plurality of packets. The DMA sequence field has a task ID unique to one DMA transfer.

In addition, as set forth in independent claim 22, the invention is a disk controller having one disk controller and another disk controller. The first disk controller includes one channel adapter having a connection interface to a host computer or a disk drive; one memory adapter for temporarily storing data to be transferred between the host computer and the disk drive; one processor adapter for controlling operations of the one channel adapter and the one memory adapter; and one switch adapter for configuring an inner network by interconnecting the one channel adapter, the one memory adapter, and the one processor adapter. The one channel adapter, the one memory adapter, the one processor adapter and the one switch adapter each include a DMA controller for performing a communication protocol control of the inner network, and packet multiplex communication is performed among the DMA controllers provided in the adapters. The other disk controller includes adapters having similar structures to structures of the one channel adapter, the one memory adapter, the one processor adapter, and the one switch adapter of the first disk controller. The one switch adapter is connected to each of said one adapters and to each of

the other adapters, and the other switch adapter is connected to each of the other adapters and to each of said one adapters.

Finally, as set forth in independent claim 24, the invention is a disk controller including a channel adapter having a connection interface to a host computer or a disk drive. A memory adapter is included for temporarily storing data to be transferred between the host computer and the disk drive. Also included are a processor adapter for controlling operations of the channel adapter and the memory adapter, and a switch adapter for configuring an inner network by interconnecting the channel adapter, the memory adapter, and the processor adapter. The channel adapter, the memory adapter, the processor adapter, and the switch adapter each include a DMA controller for performing communication protocol control of the inner network, and a data link engine for executing DMA transfer to and from the inner network. A packet to be transferred among the DMA controllers provided in the adapters includes an address field for designating a targeting DMA controller, an address field for designating an initiating DMA controller, and a DMA sequence field for managing a transfer sequence when one DMA transfer is distributed to a plurality of packets.

One of the benefits that may be derived is a disk controller using connection-less type multiplex communication, capable of addressing issues of the prior art, realizing a high transfer efficiency (performance) while retaining a high reliability equivalent to that of a conventional disk controller, and realizing a low cost.

B. Discussion of the References

In the present invention, a disk controller utilizes connection-less multiplex communication whereby multiplex becomes possible not only during one DMA sub-transfer, but also during a plurality of sub-DMA transfers. This considerably improves path-use efficiency, and eliminates the necessity of separately providing a control system inner network and a data system inner network, as in the case of a conventional disk controller. Since path use efficiency is improved, the path use limitation is relaxed so that the processor in the channel adapter can be used in a processor adapter that is independent from the channel adapter. The cache memory adapter and control memory adaptor are integrated into a single memory adapter, and a switch adapter is included for interconnecting the channel adapter, the memory adapter and the processor adapter.

These advantages of the invention are realized in the claims, in that each of the independent claims 1, 7, 8, 22, and 24 sets forth a disk controller having a channel adapter, a memory adapter, a processor adapter, and a switch adapter for configuring an inner network by interconnecting the channel adapter, the memory adapter and the processor adapter. The channel adapter, the memory adapter, the processor adapter, and the switch adapter each include a DMA controller for performing communication protocol control of the inner network. Thus, the independent claims of the present application are patentable over the prior art of record as discussed below with respect to each reference.

1. U.S. Patent No. 5,206,943

The patent to Callison, US 5206943, shows a disk array controller that includes DMA channels between a microprocessor, a bus master interface, a compatibility interface, and a buffer memory. DMA channels are also provided between the disk interface and the buffer memory. A transfer controller is included that is generally a specialized, multi-channel DMA controller used to transfer data between a transfer buffer RAM and various other devices present in the disk array controller. There are seven DMA channels present in the transfer controller, including a bus master integrated controller channel, a compatibility port channel, a local processor channel, and four DMA disk channels. (See, e.g., Abstract, figure 2, column 3, line 62, through column 5, line 49.) However, while Callison teaches multiple DMA channels in a disk array controller, Callison does not teach multiple DMA controllers that perform communication protocol control of an inner network in a disk controller, as taught by the present invention. Thus, Callison does not teach a disk controller that includes a channel adapter, a memory adapter, a processor adapter, and a switch adapter for configuring an inner network by interconnecting the channel adapter, the memory adapter and the processor adapter, wherein the channel adapter, the memory adapter, the processor adapter, and the switch adapter each include a DMA controller for performing communication protocol control of the inner network.

2. U.S. Patent No. 6,401,149

The patent to Dennin, US 6401149, shows various methods for context switching within a disk controller wherein the disk controller includes a data buffer used to buffer data transferred between a mass storage device and an I/O bus. In one embodiment,

the data buffer includes a multi-port memory that is a DMA (direct memory access) memory. The multi-port memory ports include a random access port, a FIFO access port, a register access port, and/or a buffer controller DMA port. The random access port is connected to a microprocessor interface bus that, in turn, is connected to one or more processors, such as a microprocessor and a microcontroller, as well as the FIFO access port. The arrangement allows form more efficient utilization of processors. (See, e.g., Abstract, figures 1-15, column 2 lines 35-67, column 3 lines 1-30, column 4-5.) However, Dennin does not teach multiple DMA controllers within an inner network. Accordingly, Dennin does not teach a disk controller that includes a channel adapter, a memory adapter, a processor adapter, and a switch adapter for configuring an inner network by interconnecting the channel adapter, the memory adapter and the processor adapter, wherein the channel adapter, the memory adapter, the processor adapter, and the switch adapter each include a DMA controller for performing communication protocol control of the inner network, as taught by the present invention.

3. U.S. Patent No. 6,604,155

The patent to Chong, US 6604155, shows a storage architecture employing a transfer node to achieve scalable performance. The system includes a first channel port coupled to a host computer, a second channel port coupled to a storage controller and one or more storage devices, a central processing unit (CPU) coupled to the first and second channel ports, and a memory coupled to the CPU. The transfer node receives data routing information associated with a data transfer command from the storage controller via the second channel port. The data transfer command directs a transfer of data between the host computer and the storage devices. The transfer node stores the data routing information within the memory, and routes data associated with the data transfer command between the first and second channel ports using the data routing information stored within the memory. The system includes a switch coupled to one or more storage devices, with the transfer node being coupled between the host computer and the switch, and a storage controller coupled to the transfer node. The storage controller may be coupled to the switch, or coupled directly to the transfer node. (See, e.g., Abstract, figures 1-10, column 3-4, column 5 lines 1-35, column 6 lines 30-67.) However, Chong also fails to teach multiple DMA controllers for multiple devices in an inner network. Thus, Chong does not disclose a disk controller that includes a channel adapter, a memory adapter, a processor adapter, and a switch adapter for configuring

an inner network by interconnecting the channel adapter, the memory adapter and the processor adapter, wherein the channel adapter, the memory adapter, the processor adapter, and the switch adapter each include a DMA controller for performing communication protocol control of the inner network, as in the present invention.

4. U.S. Patent Publication No. 2002/0087751 A1

The published US patent application to Chong, US 20020087751, shows a switch-based scalable performance storage architecture. The computer system includes a data switch coupled between a host computer and one or more storage devices. A storage controller for managing the storage of data within the one or more storage devices is coupled to the switch. The switch includes a memory for storing data routing information generated by the controller, and uses the data routing information to route data directly between the host computer and the one or more storage devices such that the data does not pass through the storage controller. Within the computer system, information may be conveyed between the host computer, the switch, the one or more storage devices, and the storage controller according to a two party protocol such as the Fibre Channel protocol. The system is able to achieve separation of control and data paths during data transfer operations, thereby improving scalability and efficiency. (See, e.g., Abstract, figures 1-12, paragraphs [0015]-[0026], [0042]-[0043], [0049]-[0053], [0057]-[0062].) However, Chong does not teach the present invention, including multiple DMA controllers. Accordingly, Chong does not teach a disk controller that includes a channel adapter, a memory adapter, a processor adapter, and a switch adapter for configuring an inner network by interconnecting the channel adapter, the memory adapter, and the processor adapter, such that the channel adapter, the memory adapter, the processor adapter, and the switch adapter each include a DMA controller for performing communication protocol control of the inner network.

5. U.S. Patent Publication No. 2003/0131192 A1

The published US patent application to Nakamura, US 20030131192, shows a clustering disk controller that includes a switch that holds a table that can modify a destination of a request from a host computer. The clustering disk controller includes a plurality of disk control units, connection means that connects the plurality of disk control units, channel control units installed in the disk control units, a switch installed in the

clustering disk controller and connected to the channel control units, and host computers. The switch includes a data table for holding correspondence information between a destination channel control unit, which is an access destination set by the host computer, and a channel control unit which actually transfers the access request. (See, e.g., Abstract, figures 1-26, paragraphs [0008]-[0011], [0040]-[0044], [0053]-[0058].) Thus Nakamura also does not disclose multiple DMA controllers. Accordingly, Nakamura does not teach a disk controller that includes a channel adapter, a memory adapter, a processor adapter, and a switch adapter for configuring an inner network by interconnecting the channel adapter, the memory adapter and the processor adapter, wherein the channel adapter, the memory adapter, the processor adapter, and the switch adapter each include a DMA controller for performing communication protocol control of the inner network, as in the present invention.

6. U.S. Patent Publication No. 2003/0182516 A1

The published US patent application to Fujimoto, US 20030182516, shows a storage system, that includes a plurality of disk control clusters. Each disk control cluster has one or more channel interface units having interfaces with host computers, one or more disk interface units having interfaces with disk drives, and a local shared memory unit for storing data to be read/written from/to the disk drives. The channel interface units execute data transfer between the interfaces with the host computers and the local shared memory units in response to a read/write request from the host computers. Also, the disk interface units execute data transfer between the disk drives and the local shared memory units to read or write the data. A switch is included for connecting the channel interface units in the plurality of disk control clusters, and the switch has a memory to which management information stored in a global information control unit is copied. (See, e.g., Abstract, figures 1-24, paragraphs [0019]-[0040], [0069]-[0076], [0116]-[0128].) Thus, Fujimoto teaches interconnected disk control clusters, but Fujimoto does not teach a disk controller that includes a channel adapter, a memory adapter, a processor adapter, and a switch adapter for configuring an inner network by interconnecting the channel adapter, the memory adapter and the processor adapter, wherein the channel adapter, the memory adapter, the processor adapter, and the switch adapter each include a DMA controller for performing communication protocol control of the inner network, as in the present invention.

7. U.S. Patent Publication No. 2004/0139365 A1

The published US patent application to Hosoya, US 20040139365, shows a high-availability disk control device and failure processing method for a high-availability disk subsystem. The disk control device includes a plurality of host interface modules configured to interface with a computer and a plurality of disk interface modules configured to interface with a storage device. Also included are a plurality of cache memory modules configured to temporarily store data read from or written to the storage device, and a switch network connecting the host interface modules, the cache memory modules, and the disk interface modules. The switch network includes at least one switch, and each of the host interface modules is configured to execute data transfers between the computer and the cache memory modules. Also, each of the disk interface modules is configured to execute data transfers between the storage device and the cache memory modules. Each of the host interface modules, the disk interface modules, and the cache memory modules includes identification information providing unique identification within the switch network, and DMA engines perform DMA operations to and from the cache memory. (See, e.g., Abstract, figures 1-18, paragraphs [0019]-[0024], [0046]-[0056], [0068]-[0071].) Thus, the system of Hosoya includes DMA engines affiliated with cache memories, but, Hosoya does not teach a disk controller that includes a channel adapter, a memory adapter, a processor adapter, and a switch adapter for configuring an inner network by interconnecting the channel adapter, the memory adapter and the processor adapter, wherein the channel adapter, the memory adapter, the processor adapter, and the switch adapter each include a DMA controller for performing communication protocol control of the inner network, as in the present invention.

8. U.S. Patent No. 5,974,058

This reference discloses a plurality of transmitters multiplexed to a hub through clocked serial links. Timing problems that may arise when switching between links are eliminated with a system including a group serial receiver for each link for performing serial to parallel conversion of data sent over the serial link, outputting a group clock signal based on the serial clock signal, outputting parallel data clocked by the group clock signal, and determining a data enable signal from the serial link. A select signal for determining the serial link being read by the hub selects the corresponding group clock, parallel data, and data

enable. A load control clocks the selected parallel data into a first-in, first-out buffer using the selected group clock when the selected data enable is asserted. When the selected data enable is not asserted, the load control is held in reset and, hence, is insensitive to irregularities in the selected clock signal due to switching between links. Data is clocked from the buffer by a local clock. The reference fails to teach a disk controller that includes a channel adapter, a memory adapter, a processor adapter, and a switch adapter for configuring an inner network by interconnecting the channel adapter, the memory adapter and the processor adapter, wherein the channel adapter, the memory adapter, the processor adapter, and the switch adapter each include a DMA controller for performing communication protocol control of the inner network.

9. European Patent Publication No. EP 1353264 A2

This reference disclose a disk storage system having high throughput between a disk adapter (DKA) of a disk controller (DKC) and a disk array (DA). The disk adapter (DKA) of the disk controller DKC) is connected to the disk array (DA) through switches (SW1, SW2, SW3, SW4). Data on a channel (D11, D12, D13, D14) between the switch (SW1) and a RAID group (R1) is multiplexed in the switch (SW1) to be transferred onto a channel (D01) between the switch (SW1) and the disk adapter (DKA) and data on the channel (D01) between the switch (SW1) and the disk adapter (DKA) is demultiplexed in the switch (SW1) to be transferred onto the channel (D11, D12, D13, D14) between the switch (SW1) and the RAID group (R1). A data transfer rate on the channel (D01) between the disk adapter (DKA) and the switch (SW1) is made higher than that on the channel (D11, D12, D13, D14). The reference does not teach a disk controller that includes a channel adapter, a memory adapter, a processor adapter, and a switch adapter for configuring an inner network by interconnecting the channel adapter, the memory adapter and the processor adapter, wherein the channel adapter, the memory adapter, the processor adapter, and the switch adapter each include a DMA controller for performing communication protocol control of the inner network.

10. U.S. Patent Publication No. 2003/0046460 A1

The published US patent application to Inoue, US 20030046460, is discussed in the specification of the present application at page 1, and disclose general background information on prior art storage systems. Accordingly, no further discussion of these references is believed necessary.

11. U.S. Patent No. 6,601,134

The patent to Yamagami, US 6601134, is discussed in the specification of the present application at page 1, and disclose general background information on prior art storage systems. Accordingly, no further discussion of these references is believed necessary.

Thus, from the foregoing, it is apparent that none of the above-discussed documents teach a disk controller that includes a channel adapter, a memory adapter, a processor adapter, and a switch adapter for configuring an inner network by interconnecting the channel adapter, the memory adapter and the processor adapter, wherein the channel adapter, the memory adapter, the processor adapter, and the switch adapter each include a DMA controller for performing communication protocol control of the inner network, as set forth in independent claims 1, 7, 8, 22, and 24. Accordingly, claims 1, 7, 8, 22, and 24, as well as their dependent claims, are patentable over the above-discussed documents.

(f) In view of this petition, the Examiner is respectfully requested to issue a first Office Action at an early date.

Respectfully submitted,

Chun-Pok Leung
Reg. No. 41,405

TOWNSEND and TOWNSEND and CREW LLP
Two Embarcadero Center, 8th Floor
San Francisco, California 94111-3834
Tel: 650-326-2400
Fax: 415-576-0300
Attachments
RL:rl
60450666 v1